PFC BASED INTEGRATED SEPIC-FLY BACK DUAL OUTPUT CONVERTER FED SRM DRIVE

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Abstract

This paper presents an isolated PFC converter with two symmetrical output voltages feeding switched reluctance motor (SRM) drive. The proposed converter is an integration of SEPIC (single ended primary inductor) and flyback converter. The high frequency transformer of flyback converter, provides input-output isolation in the system. Both SEPIC and flyback converters are designed for discontinuous conduction mode (DCM) of operation to obtain power factor correction at input side. The speed control of proposed drive is achieved by regulating converter output DC voltage. The proposed converter provides improved power quality over wide input voltage range and loading conditions. Experimental results of a prototype of integrated SEPIC-flyback converter fed SRM drive is demonstrated here. The obtained power quality parameters comply with given regulation for harmonics, such as IEC 61000-3-2.

Keywords*— SEPIC; Fly back; Mid-point converter; DCM; SRM; Power Quality.*

Introduction

Power factor correction (PFC) based converters are becoming popular to meet the given **IEC** standard **[1]** for power quality and energy efficiency. Small power motors are generally used in most of the domestic appliances, which adversely affect the AC mains. Thus, employing power factor correction (PFC) converter becomes necessary for the household equipment's connected to AC mains. These PFC converters increase the input power factor and decrease the total harmonic distortion (THD) of their input current. Therefore, this paper proposes a PFC based isolated converter fed low power switched reluctance motor (SRM) drive for home appliances.PFC converters bring the input current in phase with AC mains voltage. Generally, three control approaches are adopted to obtain PFC depending upon the behaviour of inductor current [2-4]. Positive inductor current throughout the complete switching period, reveals the converter operating in continuous conduction mode (CCM). Discontinuous conduction mode (DCM) refers to inductor current below zero, before end of each switching period for some time. However, in boundary conduction mode (BCM) control approach, the converter operates at the boundary between CCM and DCM. The advantage offers by the CCM of operation, is the lower root mean square (rms) current through the circuit components and the power switches, thus reducing the losses and yielding higher efficiency. However, at the expense of accurate measurement of current through the inductor operating in CCM, it requires extra current sensor and complex control. **The** PFC converter

operating in CCM also suffers from high voltage stress during light load condition as there is no direct relationship between output power and the duty cycle.

BCM exhibits combined features of both CCM and DCM of operation. The ripple current in this case, is more than CCM but lower than DCM of operation. However, just like CCM, BCM also requires one additional current sensor for detecting zero inductor current. The variable frequency operation of BCM has resulted in more complex design for EMI filter.

The DCM of operation, requires compact design of circuit inductor without any current sensing. The large permitted ripple current is the main disadvantage of the DCM operation. Therefore, higher rms current through the active and the passive circuit components, which further increases the converter losses. The absence of any current sensing has made the control simpler with reduction in converter size and cost. However, DCM also offers direct control of the power with control over duty cycle of the control switch. This direct control over duty cycle, results in fast output voltage regulation.

The high torque output for wide speed range, good fault tolerant ability, low cost over mass production, simple structure, are some of the potential advantages, which SRM has over other special electrical machines [5-6]. SRM is a dynamic electric machine converting reluctance torque into mechanical power. The torque developed in SRM, is a nonlinear function of rotor position and stator current. The control of SRM requires synchronization of phase excitation with the rotor position, therefore, to control SRM, exact rotor position determination is required. Radial vibrations in SRM, are due to sudden excitation and de-excitation, which are dominant source of vibrations and acoustic noise. Therefore, simultaneous excitation of two motor phases based control, is adopted which increases average torque and prevent complete magnetization and demagnetization of motor phases.

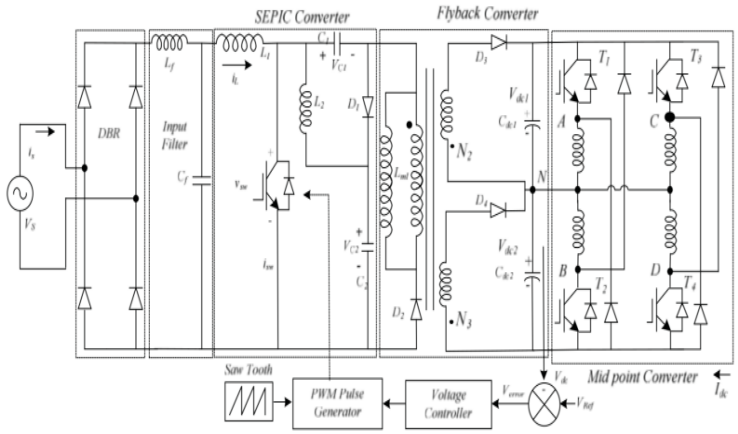


Fig. 1 Integrated SEPIC-Flyback converter fed SRM drive

PROPOSED SRM DRIVE

Fig. 1 shows the integrated-SEPIC-flyback converter fed SRM drive [7]. The isolation provides opportunity to extend similar structure for multiple output isolated converters. The proposed

converter generates dual output voltage of same magnitude, without any extra voltage balancing loop. The design of circuit magnetics is selected to operate in DCM, which reduces the size of the circuit inductors including isolation transformer. Low pass LC filter is used with filter inductor *Lf* and filter capacitor *Cf* to eliminate high frequency switching harmonics [7]. The magnetization inductance of isolation transformer $L_n a$ enters DCM first, than the input inductor *L1* and finally the intermediate inductor *L2*. Two intermediate capacitors of the circuit *CI* and *C2* are selected for CCM and DCM of operation, separately. The maximum voltage stress appearing across the device during switch off is equal to the sum of voltage across two intermediate capacitors *C1* and *C2* when diode D_1 is forward biased. Two well regulated converter output voltages are fed to a mid-point converter feeding SRM drive. However, the speed control of proposed converter fed SRM drive is achieved by controlling two equal output voltages of the proposed converter.

Integrated-Sepic Fly back Converter

The working of proposed integrated-SEPIC flyback converter is illustrated in Fig. 2, under five operating modes.

- **Mode I**: Fig. 2(a) reflects the current path during this operating mode. This mode defines the switch on state. The input inductor L_1 and transformer magnetising inductance $L_{,,,/}$ start charging through rectified input voltage Vi_n, and intermediate capacitor voltage *Vci* with the start of this operating mode. However, intermediate inductor *L2* starts discharging through intermediate capacitor voltage, *Vci*. During this mode, diode *D3* and *D4* remain in reverse biased condition, thus requirement of load current is fulfilled by two series connected DC link capacitors *Cid* and *Cda.*
- **Mode II**: Fig. 2(b) reflects the circuit operation during this operating mode. This mode begins as the switch Su gets turns off. The input inductor *L1*, intermediate inductor *L2* and transformer magnetising inductance $L_n a$ keep on discharging during this operating mode. Diode *D3* and *D4* which are reversed biased during *Mode I*, are forward biased during this operating mode. As the diode D_1 starts conducting, the voltage across switch Su is clamped to *Vci+Vc2*•
- **Mode III:** Fig. 2(c) shows the current path during this mode. This mode starts as the current through magnetising inductance L.] decreases to zero as *D2* turns off. The current through input inductor *L*, intermediate inductor *L2*, keeps on decreasing till the end of this operating mode.
- **Mode IV***:* The current through intermediate inductor *L2* becomes less than zero with the advent of this this mode. Moreover, the input inductor *L1* continues discharging through intermediate capacitor C_1 and *C2*. Fig. 2(d) reflects the circuit during this mode.
- **Mode V***:* Input inductor current decreases to zero with the start of this operating mode. In this mode diode *Di* turns of and voltage across switch decreases to V_{in} and remains at this voltage until the start of next switching cycle as shown in Fig. 2(e).

Control Algorithm

The control of proposed drive is implemented using DSP (dSPACE 1104). The developed control receives sensed DC link voltage and position encoder feedback to generate PWM signals, which are then transmitted to gate drives of PFC converter switch and split capacitor converter switches. The control of proposed converter fed SRM, is described as follows,

Control of Front-End PFC Converter

In conventional current control mode, two control loops are designed i.e., current control loop, which shapes the input current and the voltage control loop to regulate the output voltage of the converter. While in voltage control mode, only single voltage loop is required. This work utilizes a voltage mode control scheme to obtain precise regulated output voltage. The error voltage v, is obtained on comparing, V_{de} with reference voltage, *v*,f.* The pulse width modulator with fixed frequency of 20 kHz.

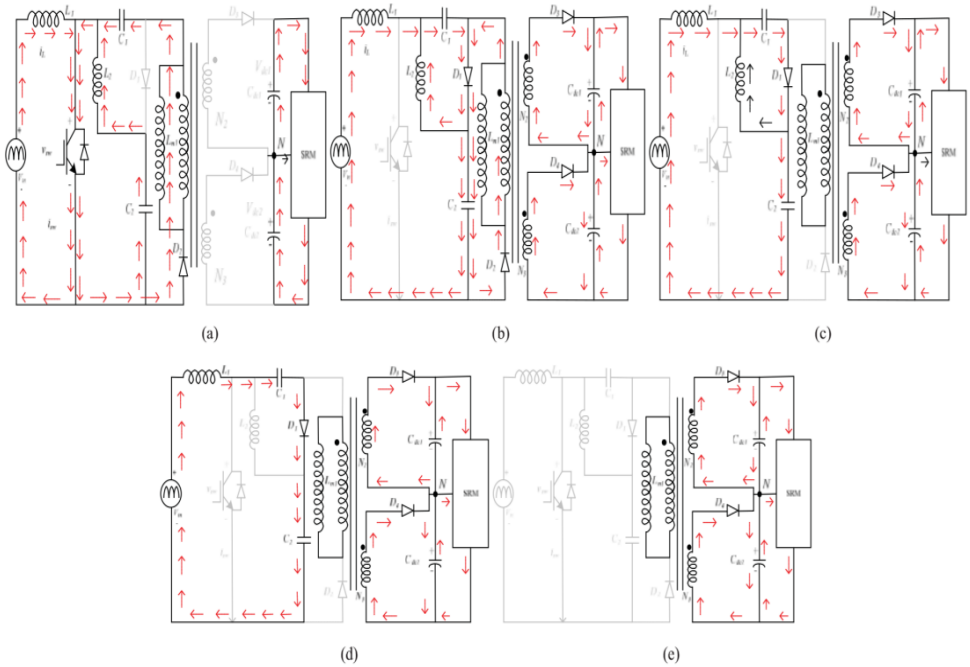


Fig. 2.Integrated SEPIC-Flyback converter operating modes (a) switch on state (Mode I), (b) switch state (Mode II), (c) Mode III, (d) Mode IV and (e) ModeV

is fed with voltage error signal to generate PWM signals for the converter. The voltage error v_e is estimated as,

$$v_e\,(u) = v_{\,ref}\,(u) — V,\,(u) \qquad (1)$$

The controlled output voltage $v_c d_c(u)$ is generated when error voltage ven-or(u) is given to a voltage proportional-integral controller, therefore vide is written as,

$$` v_{edc}\,(u) = v_{ede}\,(u —1) + k_{\,pr} f v_e\,(u) — v_{error}\,(u —1)\} \; k_{ifi}\, v_e\,(u) \qquad (2)$$

The gains for proportional plus integral controllers are denoted by k_{pr} and k_{1n}, where *(u)* is considered as sampling instant.

Control of SRM

The phase inductance in case of SRM, is not only the function of rotor position but it also the function of excitation current. Therefore, exact determination of rotor position is necessary to achieve high performance of the motor. The hysteresis current control requires determination of reference current such that motor phases are switch on and off according to hysteresis band frequency. Here, single pulse mode based control is adopted such that phases are switched on and off once during each cycle. Table-I shows applied switching pulses to a midpoint converter switches *T1, T2, T3* and *Ti* to excite two motor phases at any instant.

Table-1 Switching Sequence

Feedback Signal		SRM Converter Switches			
A	B	T,	T2	T_3	T4
o	o	1	1	0	0
o	i	0	1	1	0
1	0	0	0	1	1
1	1	1	0	0	1

Performance of Proposed Converter Fed SRM Drive

To examine the performance of integrated SEPIC-flyback converter with two symmetrical output voltages feeding SRM drive, the prototype is designed and implemented in the laboratory. The proposed SRM drive is coupled to a DC generator feeding a resistive load bank. The SRM is fed with the mid-point converter having arrangement of one switch and one diode for each phase. The pulse width modulated pulses for the midpoint converter and proposed PFC converter, are generated using DSP-dSPACE-1104. The experimental results are explained as follows.

Steady State Performance

Two phase windings of SRM are excited simultaneously to reduce acoustic noise and decrease torque ripple in proposed SRM drive, which is shown in Fig. 3(a). Fig. 3(b) demonstrates *V dc* as 150 V and the two equal output voltages *Vder* and *Vdc2* across the mid-point converter capacitors as 75 V each. As expected, the voltages across two output capacitors Vd_c3 and *Vdc2* are equal in magnitude without any voltage balance loop. Fig. 3(c) shows the operation of drive at rated *Vdc* and rated phase current with improved power quality at input side. To obtain the reduced speed operation of proposed SRM drive, the *V* is maintained as 50 V. Fig. 3(d) demonstrates the high power factor operation of proposed PFC converter fed SRM drive with reduced input current THD at low speed.

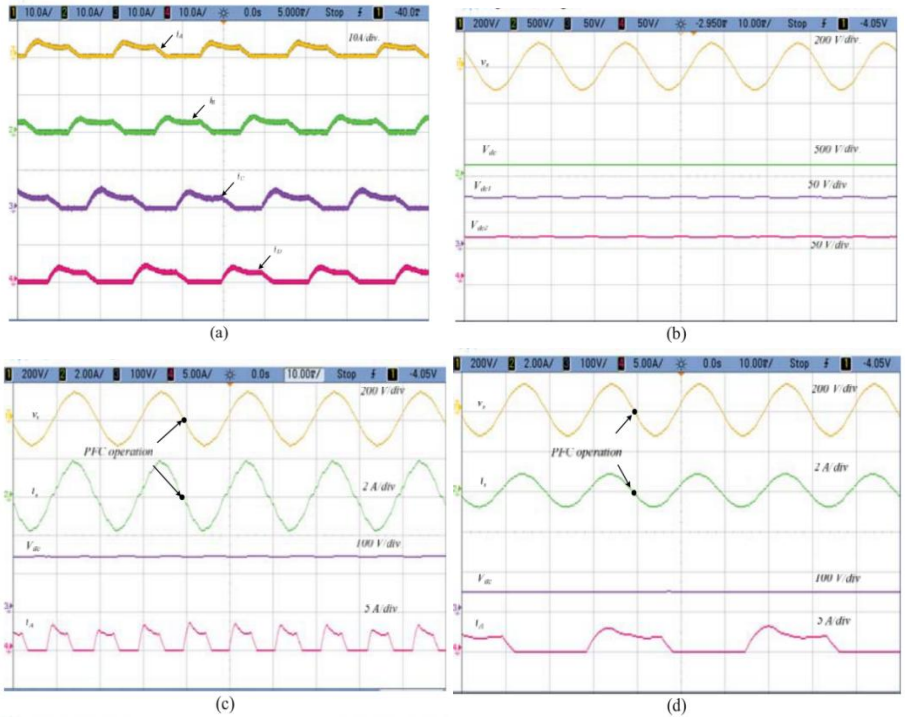
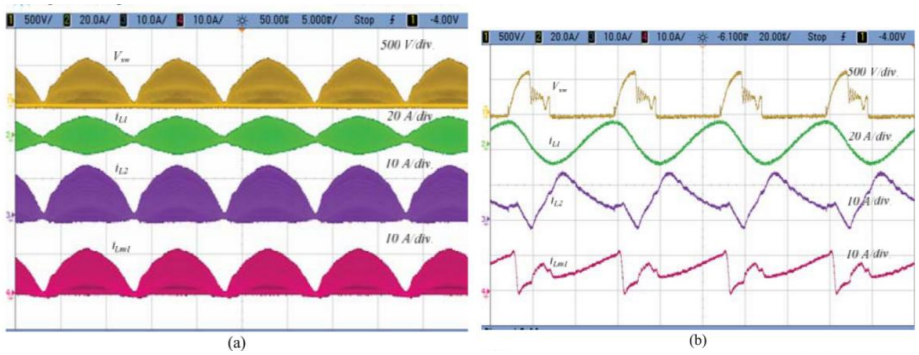


Figure 3 Experimental results : (a) Motor Current (b)two Symmetrical output Voltages (c) improved Power quality operation at V_{dc} as 150V and (d) at V_{dc} as 50V

Performance of Proposed Converter

The CCM and DCM voltages and currents across different circuit components as per the selected design, are shown in Fig. 4. All the three inductors including input inductor L_1, intermediate inductor ***L2*** and inductance of isolation transformer $L_{,,i}r$ are selected to operate in DCM, which is shown in Fig. 4(a). The intermediate capacitor Ci operates with continuous voltage across it whereas capacitor *C2* operates with discontinuous voltage across it during each switching period, which is reflected in Fig. **4(b).** Fig. 4(c) shows the current through diode ***D3*** and *D4* during switch off state.



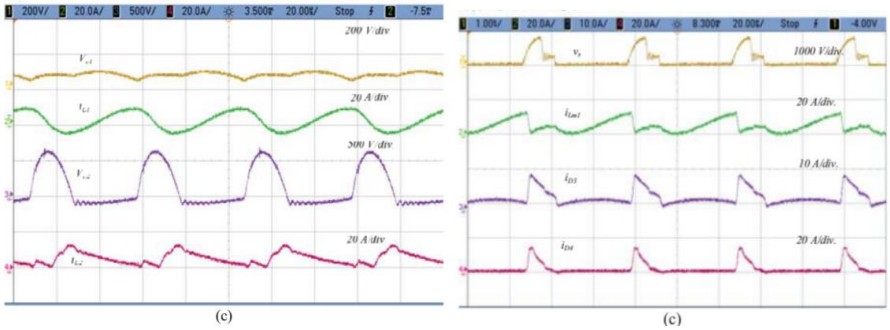
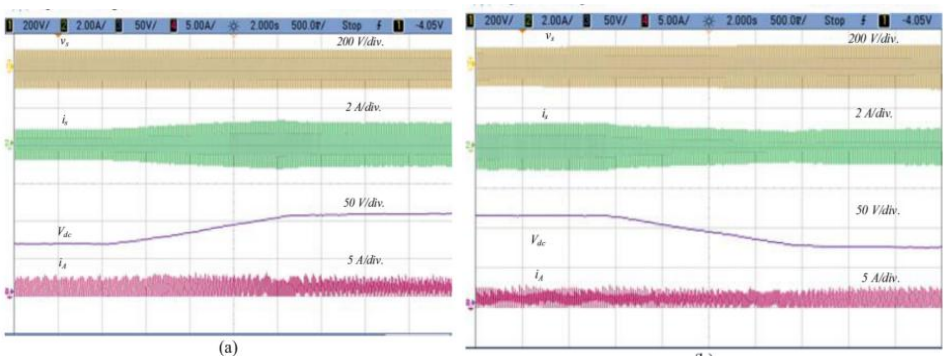
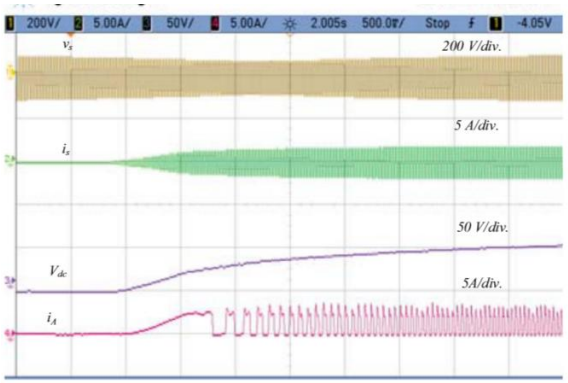


Figure 4 Experimental wave from showing (a) current through input inductor L_1,intermediate inductor L_2 and current through magnesting inductance Lm_1 during each swithing period, (b) Zoomed view of fig (a),(b) voltage across C_1, and C_2 and (c) current through diode D_3 and D_4 during each switching period

Drive During Dynamic Conditions

The proposed low power SRM drive with improved power quality is tested under different dynamics conditions, which is shown in Fig. 5. Very fast speed control and smooth dynamic transition, are observed in the proposed drive when ***Vdc*** is controlled from 70 V to 120 V DC, which is reflected in Figs. 5(a). Similarly performance of the proposed drive during change in ***Vd0*** from 130V to 80V is shown in Fig. 5(b). In Fig. 5(a) and (b), the change in motor phase current frequency is observed, which demonstrates the change in motor speed with an increase or decrease in ***Vdc*** of the SRM drive. Fig. 5(c) presents the starting dynamic with $\boldsymbol{Vd_e}$ as 50V such that drive input current is well under limit.





(c)

Fig.5 Experimental results with variation in V_{dc} from: (a) 70 V to 120V (b) 130 V to 80 V and (c) Dynamic during starting

Power Quality Performance

The proposed SRM drive is subjected to different supply voltage fluctuations and wide output voltage change. However, input current THD obtained under all the test conditions comply with the given IBC standard [1]. Based on the measured current harmonics, the THD is recorded as 5.8%, at rated speed operation of integrated SEPIC-flyback converter fed SRM drive with Vdc as 150 V and V_8 as 90 V, which is shown in Figs. 6(a)-(c). The current THD is observed as 9% when Vs is considered as 110 V, which is shown in Figs.6(d)- (f).Similarly the power quality results are recorded with V& as 50V and THD as 3.5%,which is shown in Figs.6(h)-(i).

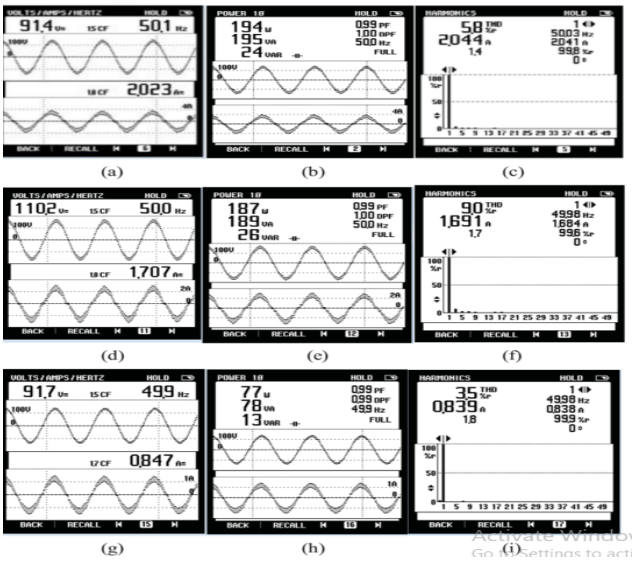


Figure 6 Power analyzer results with (a)-(c) V_{ac} = 90 V and V_{dc}= 150V (d)-(f) V_{ac} = 110 V and V_{dc}= 150V and (g)-(i) V_{ac} = 90 V and V_{dc}= 50V

Conclusions

An isolated dual output PFC converter fed SRM drive has been demonstrated here. The proposed converter provides PFC and produces well control two symmetrical output voltages. All the circuit inductors are selected to operate in DCM, which have reduced the size, cost and control complexity of the proposed drive. It can be seen that power factor is higher than 0.99 and obtained input current THD is low for all tested cases. According to experimental results, proposed drive performance is satisfactory under different input voltage variation and loading conditions. Moreover, obtained results of drive show the smooth transient operation and fast speed control.

Appendix

Motor rating: 200 W, 8/6 pole, 1500rpm, L_i, = 12mH, L_a = 110mH, R= 0.751, J = 0.016kg m^2, B = 0.0065Nms: Ca,/ =*Cdc2* = 1000 piF. Input voltage: 14, 90V, 50 Hz, $K_{,,}$ = 0.008;
Ki_n = 0.0008, Li=470p,H, L2=250j.tH, Cr=10, C2=200nF and Lna=188p,H.

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